AMENDMENTS TO THE CLAIMS:

Claim 1. (Currently amended) In a display system comprising an array of pixel cells formed on a substrate, wherein each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate, a device comprising:

a first and second transistor formed on said substrate each transistor comprising ~~having~~ a gate electrode and first and second electrodes defining a serpentine channel region there between.

Claim 2. (Previously presented) The device of claim 1, wherein a common electrode comprises one of said first and second electrodes of said first transistor and one of said first and second electrodes of said second transistor.

Claim 3. (Currently amended) The device of claim 1, wherein said first transistor is coupled between a gate line and a probe pad formed on said substrate and selectively couples said probe pad to said gate line during a test routine whereby a charge is written to, stored, and read from said array of pixel cells.

Claim 4. (Currently amended) The device of claim 1, wherein said first transistor is coupled between a data line and a probe pad formed on said substrate and selectively couples said probe pad to said data line during a test routine whereby a charge is written to, stored, and read from said array of pixel cells.

Claim 5. (Currently amended) The device of claim 1, wherein said second transistor is coupled between a gate line and a probe pad formed on said substrate and selectively couples said probe pad to said gate line during a test routine whereby a charge is written to, stored, and read from said array of pixel cells.

Claim 6. (Currently amended) The device of claim 1, wherein said second transistor is coupled between a data line and a probe pad formed on said substrate and selectively couples said probe pad to said data line during a test routine whereby a charge is written to, stored, and read from said array of pixel cells.

Claim 7. (Previously presented) The system of claim 1, wherein said first transistor comprises a select transistor and is connected to a first probe pad and a gate select control pad and wherein said second transistor comprises a hold transistor and is connected to a second probe pad and a gate hold control pad.

Claim 8. (Previously presented) The system of claim 7, wherein said select transistor and said hold transistor are connected by a common electrode to at least one of said plurality of gate lines.

Claim 9. (Currently amended) The system of claim 7, wherein said select transistor and said hold transistor are connected ~~to~~ by a common electrode to at least one of said plurality of

data lines.

Claim 10. (Previously presented) A display system comprising an array of pixel cells formed on a substrate, wherein each pixel cell is coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate, the system comprising:

a gate line select/hold circuit formed on said substrate and connected to at least one of said plurality of gate lines, a first control pad and a first probe pad; and

a data line select/hold circuit formed on said substrate and connected to at least one of said plurality of data lines, a second control pad and a second probe pad, wherein at least one of the gate line select/hold circuit and the data line select/hold circuit comprises first and second transistors each having first and second electrodes defining a serpentine channel region.

Claim 11. (Previously presented) The system of claim 10, wherein said gate line select/hold circuit is connected to a set of said plurality of gate lines.

Claim 12. (Previously presented) The system of claim 10, wherein said data line select/hold circuit is connected to a set of said plurality of data lines.

Claim 13. (Previously presented) The system of claim 10, wherein said gate line select/hold circuit is connected to a plurality of first control pads.

Claim 14. (Previously presented) The system of claim 10, wherein said data line select/hold circuit is connected to a plurality of second control pads.

Claim 15. (Previously presented) The system of claim 10, wherein said gate line select/hold circuit includes a select logic and a hold logic.

Claim 16. (Previously presented) The system of claim 10, wherein said data line select/hold circuit includes a select logic and a hold logic.

Claim 17. (Previously presented) The system of claim 10, wherein said gate line select/hold circuit is connected to a third probe pad and third control pad.

Claim 18. (Previously presented) The system of claim 17, wherein said gate line select/hold circuit comprises:

a select logic connected to said first probe pad and to a plurality of said first control pads; and

a hold logic connected to said third probe pad and to a plurality of said third control pads.

Claim 19. (Previously presented) The system of claim 10, wherein said data line select/hold circuit is connected to a third probe pad and third control pad.

Claim 20. (Previously presented) The system of claim 19, wherein said data line select/hold circuit comprises:

a select logic connected to said second probe pad and to a plurality of said second control pads; and

a hold logic connected to said third probe pad and to a plurality of said third control pads.

Claim 21. (New) A display comprising an array of pixel cells formed on a substrate, the display comprising:

a first and second transistor formed on said substrate, each transistor comprising a gate electrode and first and second electrodes which define a serpentine channel region.

Claim 22. (New) The display of claim 21, wherein each pixel cell is coupled to at least one gate line of a plurality of gate lines and at least one data line of a plurality of data lines.

Claim 23. (New) The display of claim 21, wherein at least one of said first and second transistors comprises a thin-film transistor.

Claim 24. (New) The display of claim 21, wherein the first and second transistors are connected in parallel.

Claim 25. (New) The display of claim 21, wherein at least one of said first and second

transistors comprises a bottom gate structure.

Claim 26. (New) The display of claim 21, wherein at least one of said first and second transistors comprises a top gate structure.

Claim 27. (New) The display of claim 21, wherein one of said first and second electrodes comprises an electrode that is shared with both of said first and second transistors.

Claim 28. (New) The display of claim 21, wherein the length of one of the serpentine channel regions is longer than the other serpentine channel region.

Claim 29. (New) The display of claim 21, wherein the serpentine channel region for each of said first and second transistors minimize the ON resistance of each of said first and second transistors.